Appl. No. 10/603,358

IN THE CLAIMS

1. - 9. (Cancelled)

10. (Currently Amended) A selective etch shallow trench isolation barrier integrated circuit chip fabrication process comprising the steps of:

forming a shallow trench space in a wafer;

depositing a selective etch isolation material in a **the** shallow trench space ~~of a device layer~~ to **fill the shallow trench space and to** form a selective etch shallow trench isolation barrier;

fabricating an intermetal dielectric layer on **the wafer such that the intermetal dielectric layer is disposed in direct contact with the selective etch isolation material in the shallow trench space** ~~top of said device layer~~;

etching a contact hole in said intermetal dielectric layer down to said selective etch shallow trench isolation barrier **such that at least a portion of the selective etch isolation material is exposed**; and

filling said contact hole with conductive material;

wherein the selective etch isolation material and the intermetal dielectric layer are formed of different materials having different etch characteristics, such that the selective etch isolation material may be exposed to the intermetal dielectric layer etching without having any significant amount of the selective etch isolation material etched away.

11. (Currently Amended) The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 10 in which said etching of said contact hole in said intermetal layer down to said selective etch shallow trench isolation barrier is a single

film layer etch step stopping on selective etch isolation material of said ~~the~~ selective etch shallow trench isolation barrier.

12. (Original) The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 11 in which said intermetal dielectric layer comprises oxide and said single film layer etch step is performed by Ar, CF_4, CHF_3, CO, and/or C_4F_8.

13. (Cancelled)

14. (Original) The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 10 wherein said selective etch isolation material includes silicon nitride or oxynitride.

15. (Currently Amended) The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 10 further comprising the steps of:

depositing the selective etch isolation material to fill said shallow trench; and

removing excess selective etch isolation material by a chemical mechanical polishing (CMP) process.

16. (Currently Amended) A **The** selective etch ~~material~~ shallow trench isolation barrier integrated circuit chip fabrication **process** of Claim 10 further comprising the steps of:

pre-cleaning a wafer using high purity, low particle chemicals;

heating said wafer;

exposing said wafer to ultra-pure oxygen in a diffusion furnace under carefully controlled conditions; and

forming a silicon dioxide film of uniform thickness on the surface of the wafer.

17. (Currently Amended) A selective etch shallow trench isolation barrier integrated circuit chip fabrication process comprising the steps of:

applying layers of oxide and nitride **to a wafer**;

creating a resistive mask pattern;

etching a shallow trench space;

depositing a selective etch isolation material in said shallow trench space to **fill the shallow trench space and to** form a selective etch shallow trench isolation barrier;

fabricating an intermetal dielectric layer **on the wafer such that the intermetal dielectric layer is disposed in direct contact with the selective etch isolation material in the shallow trench space**;

etching a contact hole in said intermetal dielectric layer down to said selective etch shallow trench isolation barrier **such that at least a portion of the selective etch isolation material is exposed**; and

filling said contact hole with conductive material;

wherein the selective etch isolation material and the intermetal dielectric layer are formed of different materials having different etch characteristics, such that the selective etch isolation material may be exposed to the intermetal dielectric layer etching without having any significant amount of the selective etch isolation material etched away.

18. (Original) The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 17 in which said etching of said contact hole in said intermetal dielectric layer down to said selective etch shallow trench isolation barrier is a single film

layer etch step stopping on selective etch isolation material of said the selective etch shallow trench isolation barrier.

19. (Cancelled)

20. (Original) The selective etch shallow trench isolation barrier integrated circuit chip fabrication process of Claim 17 wherein said selective etch isolation material includes silicon nitride or oxynitride.